Power Electronic Transformer with Reduced Number of Switches: Analysis of Clamp Circuit for Leakage Energy Commutation

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***Abstract*—High frequency linked ac/ac converters are important in harnessing energy from renewable energy sources and connecting them to the high voltage ac grid. Theoretically, these converters provide single stage power conversion and obviates the need for any storage elements. Any switching transition in the load side converter causes overvoltages due to the presence of non-ideal leakage inductances in the windings of the high frequency transformer. A clamp circuit is needed for commutation of this leakage energy and to protect the power electronic devices. This paper provides a detailed analysis of the power loss incurred in the clamp circuit along with a method to design the clamp components. The entire circuit has been simulated along with non-ideal leakage inductance and the presented simulation results confirm the analytical predictions.**

I. Introduction

Transformers are an integral part of power conversion systems because they provide galvanic isolation along with voltage transformation. At low operating frequencies, however, it is one of the heaviest and most expensive component in these systems. Replacing these line-frequency transformers with Power Electronic Transformers (PET) will lead to reduction in weight and volume and consequently in cost of copper and iron. These topologies are especially attractive for wind power generation systems. A survey of various multi-stage PET's that use reactive components are presented in [1].

A review of high frequency transformer linked ac/ac topologies with single-stage power conversion, bidirectional power flow and power factor correction are given in [2]. Lossless source-based commutation of leakage energy is possible in a number of these topologies [2], [3]. They employ many switches and have relatively complicated switching strategy.

A high frequency transformer (HFT) linked three phase ac/ac topology (Fig. 1) was proposed in [4]. This topology has only two switches on the primary side which is generally the high voltage side. Source base commutation is not possible in this topology however a new modulation technique is proposed in [5] that takes care of the primary leakage inductance problem. A secondary side clamp circuit is still necessary. This paper presents a detailed analysis of secondary side leakage energy commutation for this topology with respect to the modulation method proposed in [5]. The power loses associated with the clamp circuit operation, the commutation time required and the voltage loss incurred are analytically calculated and checked with simulation. The analysis developed in this paper is quite general and is applicable to analysis of the clamp circuit in topology B2 and B3 in [2].

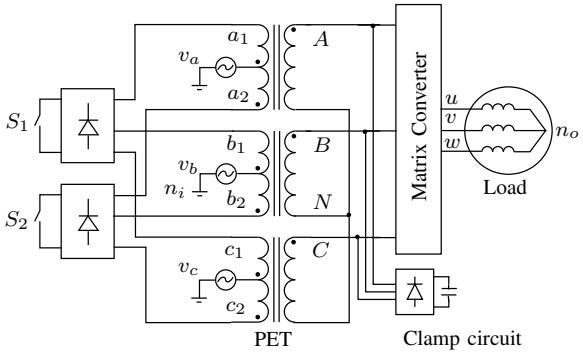

Fig. 1. Topology

II. Introduction to the topology

A brief description of the topology in Fig. 1 as well as its operation is given in this section for a better understanding of the analysis in the subsequent sections. In this topology, three phase balanced voltages are fed to a set of three three-winding transformers as shown in Fig. 1. The switches S_1 and S_2 are switched at a high frequency (f_s) and constant duty ratio of 50%. When S_1 is ON, terminals a_1, b_1 and c_1 are connected to form a star point making the secondary voltages in phase with the primary voltages. When S_2 is ON, terminals a_2, b_2 and c_2 form a star point and the secondary voltages are in phase opposition with the input voltages. In this way, the three phase balanced low frequency input voltages are converted to high frequency voltages at the secondary side of the transformer and the flux is balanced over one switching interval. The primary voltage v_a for phase a along with the corresponding secondary side high frequency waveform v_{AN} is shown in Fig. 2. This high frequency voltage is unfolded into a adjustable frequency and voltage waveform using a matrix converter.

In a matrix converter, there are 27 permissible switching states. Six of these switching states generate synchronously rotating space vectors (active vectors) [6]. Based on the direction of rotation, these six vectors are further divided into three clockwise (cw) and three counter-clockwise rotating (ccw) vectors. The vector diagrams for ccw and cw rotating vectors are shown in Fig. 3 and Fig. 4 respectively; where the bold lines are the vectors when S_1 is ON and the dashed lines represent the vectors when S_2 is ON. Using any two adjacent vectors (either ccw or cw) and zero vectors, the output voltage can be synthesized and a modulation index of upto 0.5 can be obtained. Modulation index is defined as the ratio of peak output voltage to peak input voltage. A modulation index of upto 0.75 can be attained using a technique described in [7]. A combination of ccw and cw rotating vectors can be used for power factor control [8].

A new modulation strategy is proposed in which S_1 and S_2 are switched when a zero vector is applied in the secondary side matrix converter [5]. When a zero vector is applied, the output currents freewheel through the matrix converter and the transformer currents are brought to zero with the help of the secondary side clamp circuit, hence S_1 and S_2 are soft switched (ZCS) and the primary clamp circuit is no longer necessary. In one cycle, the output voltage is synthesized using ccw rotating vectors, and in the following cycle, cw rotating vectors are used in order to get unity power factor. In a switching cycle, the reference voltage vector is in one of the six sectors. The two adjacent active vectors that form that particular sector are used to generate the output voltage. Say, the reference vector, $\vec{V}_{ref}$ is in sector 1 (Fig. 3), the duty ratios d_1 and d_2 for these two active vectors $\vec{V}_1$ and $\vec{V}_2$ respectively are compared with a triangle waveform having a peak value of $\hat{V_{tri}}$ to obtain the switching pulses p_{V_1} and p_{V_2} as shown in Fig. 5. A zero vector is applied for the remaining time period. The switching pulse for the zero vector is p_z. Whenever there is a change in switching state of the matrix converter, the currents through the non-ideal leakage inductances of the transformer are interrupted and the secondary clamp circuit provides a path for these currents to flow. The clamp circuit is operational four times each switching cycle, for two zero

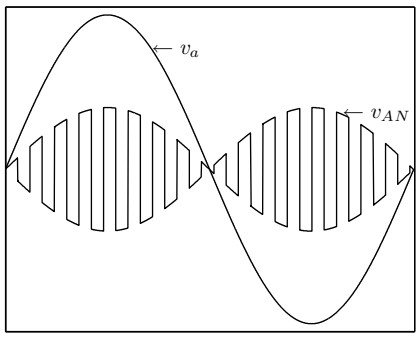

Fig. 2. Primary and secondary phase voltages

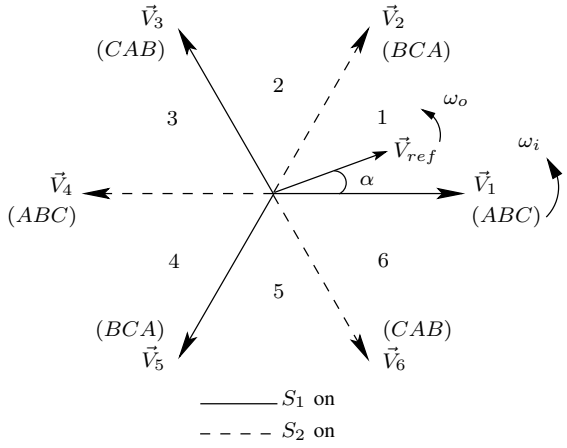

Fig. 3. ccw rotating vectors

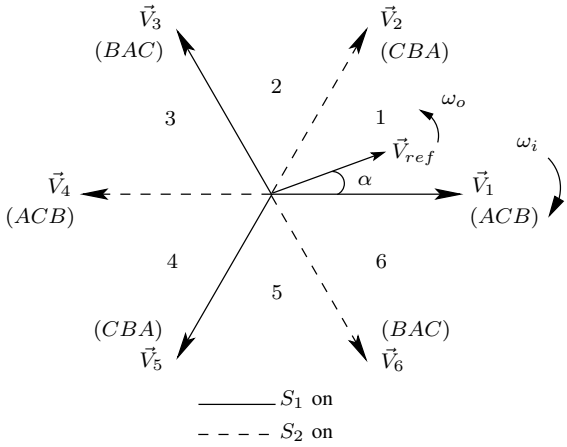

Fig. 4. cw rotating vectors

vector to active vector transitions (t_{za1}, t_{za2}) and remaining two for active vector to zero vector transitions (t_{az1}, t_{az2}). From here on, the clamp circuit refers to the secondary side clamp circuit. This secondary clamp circuit consists of a diode bridge connected to a capacitor. The power extracted from the clamp circuit is supplied to the auxiliary control circuits. For simplicity here, the clamp capacitor is replaced by a dc voltage source of magnitude V_{clp}. The diodes in the clamp circuit are considered to be fast acting so they come into conduction almost instantaneously.

III. Clamp Circuit Analysis

In this analysis, the turns ratio of the three winding transformers are assumed to be unity, and the leakage inductance of each winding is L. Also, the commutation time intervals are small compared with the switching period. The input three phase balanced voltages have a peak value of V and a frequency of ω_i rad/sec and are given by (1). Neglecting the switching ripple, the output current can be represented by (2), where, I is the peak value of output current and ω_o is the

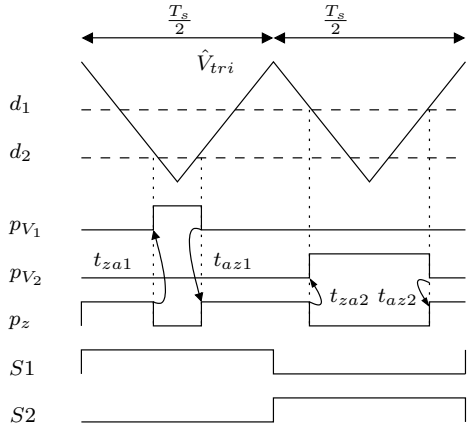

Fig. 5. Switching pulses

frequency in rad/sec.

$$\begin{aligned} v_a(t) &= V\cos(\omega_i t) \\ v_b(t) &= V\cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ v_c(t) &= V\cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{aligned} \tag{1}$$

$$\begin{aligned} i_u(t) &= I\cos(\omega_o t - \phi) \\ i_v(t) &= I\cos\left(\omega_o t - \frac{2\pi}{3} - \phi\right) \\ i_w(t) &= I\cos\left(\omega_o t + \frac{2\pi}{3} - \phi\right) \end{aligned} \tag{2}$$

In this section the operation of the secondary clamp circuit is analyzed for 1) an active to zero vector transition and 2) a zero to active vector transition. Depending on the polarity of output currents, each of these transitions has two special cases, a) when two out of three currents are positive and b) when two out of three phase currents are negative. Hence, each transition is studied when $\omega_o t$ is between $-\pi/6$ and $\pi/6$ and when $\omega_o t$ is between $\pi/6$ and $\pi/2$. The analysis for these commutation intervals when S_2 is ON, are the same as for the commutation intervals when S_1 is ON, except that the input voltage polarities are reversed, hence, the analysis when S_1 is ON is sufficient.

As the switching frequency is much higher than the fundamental frequency, in one switching cycle, the output currents and the input phase voltages can be considered to be dc. The output phase currents are assumed to be constant current sources of values I_u, I_v and I_w. As synchronously rotating vector are used in the modulation, each output terminal of the matrix converter is connected to a unique input terminal, leading to six possible combinations. When an active vector is applied, for generality, the input voltage connected to phase u, v and w are denoted by v_u, v_v and v_w respectively. For a given choice of output currents, the power loss and commutation time depends on the input voltage. This dependence can be observed by plotting the clamp power loss or the commutation time required for all combinations of input voltages. In the last part of this section, the voltage loss incurred due to operation of clamp circuit is calculated.

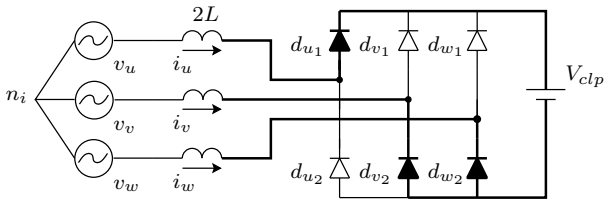

Fig. 6. Active vector to zero vector equivalent circuit

A. Active to Zero Vector Transition

When a zero vector is applied in the matrix converter, the output currents freewheel through the matrix converter and the clamp circuit will provide a path for the leakage currents to flow. Without loss of generality, let us analyze the case when S_1 is ON and a zero vector is applied (t_{az1}). Neglecting the magnetizing current, the transformer can be represented by its series leakage inductance ($2L$) only. Say i_u is positive and i_v and i_w are negative (i.e $-\pi/6 \leq \omega_o t \leq \pi/6$). The instantaneous values of phase currents i_u, i_v and i_w when the zero vector is applied are denoted by I_u, I_v and I_w respectively. The positive direction of current in phase u forces diode d_{u_1} to conduct. Similarly, diodes d_{v_2} and d_{w_2} will conduct. The equivalent circuit when the clamp circuit is operational is drawn in Fig. 6.

The KVL equation for the loop containing v_u, $2L$, d_{u_1}, V_{clp}, d_{v_2}, $2L$ and v_v is given by (3). Similarly, the KVL loop containing v_u, $2L$, d_{u_1}, V_{clp}, d_{w_2}, $2L$ and v_w is given by (4). The KCL equation for currents at node n_i results in (5).

$$v_u - 2L\frac{d}{dt}i_u - V_{clp} + 2L\frac{d}{dt}i_v - v_v = 0 \tag{3}$$

$$v_u - 2L\frac{d}{dt}i_u - V_{clp} + 2L\frac{d}{dt}i_w - v_w = 0 \tag{4}$$

$$\frac{d}{dt}i_u + \frac{d}{dt}i_v + \frac{d}{dt}i_w = 0 \tag{5}$$

The above three equations can be solved to obtain the rate of change of phase currents (6) - (8)

$$\frac{d}{dt}i_u = \frac{3v_u - 2V_{clp}}{6L} \tag{6}$$

$$\frac{d}{dt}i_v = \frac{3v_v + V_{clp}}{6L} \tag{7}$$

$$\frac{d}{dt}i_w = \frac{3v_w + V_{clp}}{6L} \tag{8}$$

The currents i_u, i_v and i_w are flowing with rates defined by equations (6) - (8). Depending on the values of t_v and t_w from Table I, either i_v or i_w will become zero amperes. In this case, let current i_v reaches zero amperes first. Diode d_{v_2} will stop conducting and equation (3) is no longer involved. Solving for the new rate of change of currents, to obtain (9).

$$\frac{d}{dt}i_u = -\frac{d}{dt}i_w = \frac{v_u - v_w - V_{clp}}{4L} \tag{9}$$

Once the initial value of current as well as rate of change of currents is known, the total time required (t_{ct}) for all the phase currents to become zero can be calculated. For this case, the current that flows into the clamp circuit is the same as i_u. The power loss in the clamp circuit can be calculated by (10), where $< i_u >_{t_{ct}}$ is the average value of current i_u during the commutation interval t_{ct}. The clamp circuit power loss for the case when i_w reaches zero before i_v can be found by interchanging I_v with I_w and v_v with v_w in (10).

$$P_{Clamp} = V_{clp} < i_u >_{t_{ct}} = \frac{V_{clp} f_s L}{2}\left[-\frac{(I_u - I_w)^2}{v_u - v_w - V_{clp}} + \frac{3I_v^2}{3v_v + V_{clp}}\right] \quad (10)$$

A similar analysis is done when S_1 is ON and i_u and i_v are positive and i_w is negative ($\pi/6 \leq \omega_o t \leq \pi/2$). The power loss for interval t_{za1} when i_v reaches zero first is given in (11).

$$P_{Clamp} = V_{clp} < i_w >_{t_{ct}} = \frac{V_{clp} f_s L}{2}\left[-\frac{(I_u - I_w)^2}{v_u - v_w - V_{clp}} + \frac{3I_v^2}{-3v_v + V_{clp}}\right] \quad (11)$$

From the above analysis, it is clear that as long as the clamp capacitor voltage is maintained higher than three times the peak line to neutral voltage, the currents will change in the desired manner. If one of the currents reach zero, the other two currents flow at a different rate and eventually become zero. The power loss in the clamp circuit is proportional to switching frequency, leakage inductance and the instantaneous values of phase currents and voltages. The value of V_{clp} is selected to be $5 \times V$. For selected values of output currents, the the per unit power loss is plotted as $\omega_i t$ is varied from 0 to 2π in Fig. 7 and Fig. 8. One per unit value is equal to $0.5LI^2 f_s$ Watts. It is observed that the power loss for the case when $-\pi/6 \leq \omega_o t \leq \pi/6$ is bound between the curves corresponding to $\omega_o t = -\pi/6$ and $\omega_o t = \pi/6$. When $\pi/6 \leq \omega_o t \leq \pi/2$, the clamp power loss is bounded by the power loss curves corresponding to $\omega_o t = \pi/6$ and $\omega_o t = \pi/2$. From the graph, the peak value of power that goes into the clamp circuit is 4.6 per unit and the minimum value is 2.2 per unit.

Table I lists the commutation time for an active to zero vector transition for different cases of output currents. The per unit time required is plotted in Fig. 9 for five selected values for output current for different combinations of input voltages. The maximum commutation required is equal to 1.06 p.u., where one p.u. equals LI/V.

B. Zero Vector to Active Vector Transition

A similar analysis is done for the transition from a zero vector to an active vector when switch S_1 is ON (t_{za1}). Consider the currents in the transformer windings are zero, when an active vector is applied in the matrix converter such that phase u, v and w are connected to phase voltages v_u, v_v and v_w respectively. In one switching cycle, the output currents can be assumed to be constant and are given by I_u, I_v and I_w for phase u, v and w respectively. The clamp circuit is active until the transformer currents match the value of the output currents. For the case when current I_u is positive and

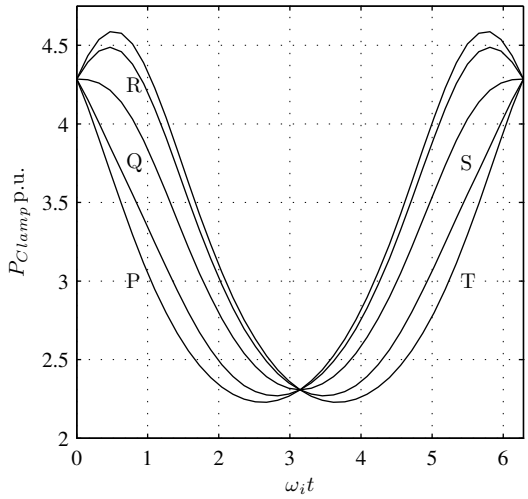

Fig. 7. Clamp circuit power loss : Active to zero vector $\omega_o t$(rads)= $-\frac{\pi}{6}$ (P), $-\frac{\pi}{12}$ (Q) , 0 (R), $\frac{\pi}{12}$ (S) and $\frac{\pi}{6}$ (T)

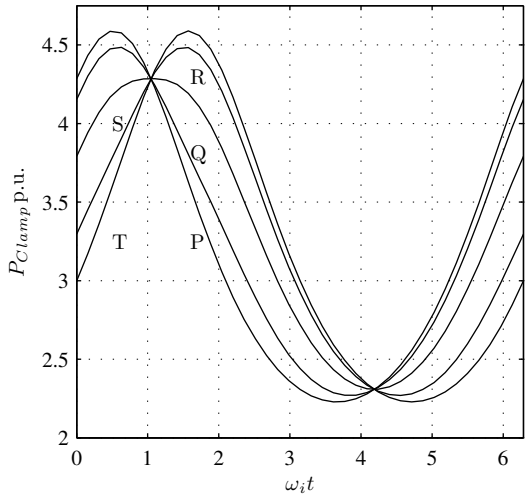

Fig. 8. Clamp circuit power loss : Active to zero vector $\omega_o t$(rads) = $\frac{\pi}{6}$ (P) , $\frac{\pi}{4}$ (Q), $\frac{\pi}{3}$ (R), $\frac{5\pi}{12}$ (S) and $\frac{\pi}{2}$ (T)

TABLE I
COMMUTATION TIME (ACTIVE TO ZERO, S_1 ON)

Output currents	time	Total time (t_{ct})
$-\frac{\pi}{6} \leq \omega_o t \leq \frac{\pi}{6}$	$t_v = -\frac{6LI_v}{3v_v + V_{clp}}$ $t_w = -\frac{6LI_w}{3v_w + V_{clp}}$	$= -2L\frac{(I_u - I_w)}{v_u - v_w - V_{clp}}$ for $t_v \leq t_w$ $= -2L\frac{(I_u - I_v)}{v_u - v_v - V_{clp}}$ otherwise
$\frac{\pi}{6} \leq \omega_o t \leq \frac{\pi}{2}$	$t_v = -\frac{6LI_v}{3v_v - V_{clp}}$ $t_u = -\frac{6LI_u}{3v_u - V_{clp}}$	$= -2L\frac{(I_u - I_w)}{v_u - v_w - V_{clp}}$ for $t_v \leq t_u$ $= -2L\frac{(I_v - I_w)}{v_v - v_w - V_{clp}}$ otherwise

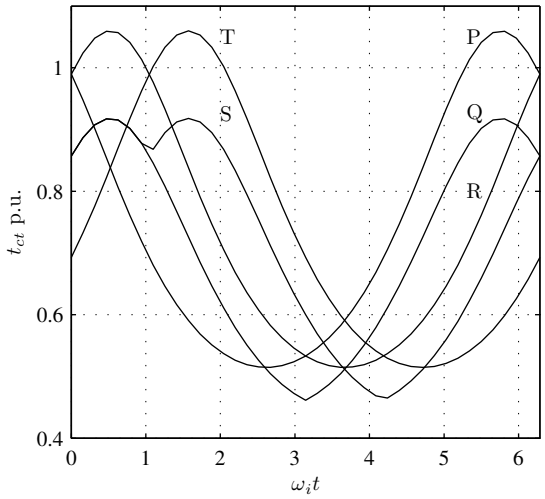

Fig. 9. Commutation time required: Active to zero vector $\omega_o t$ (rads)= $-\frac{\pi}{6}$ (P), 0 (Q) , $\frac{\pi}{6}$ (R), $\frac{\pi}{3}$ (S) and $\frac{\pi}{2}$ (T)

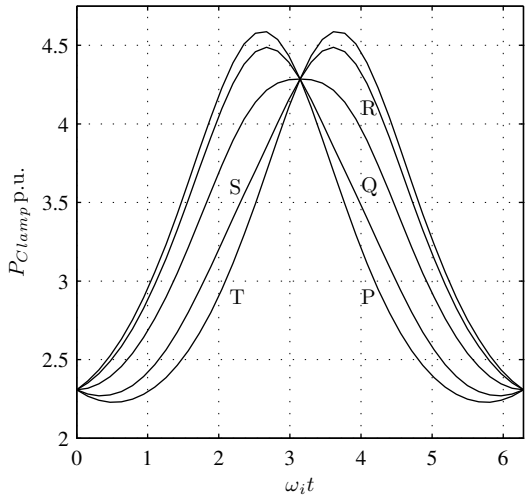

Fig. 11. Clamp circuit power loss : Zero to active vector $\omega_o t$ (rads)= $-\frac{\pi}{6}$ (P), $-\frac{\pi}{12}$ (Q) , 0 (R), $\frac{\pi}{12}$ (S) and $\frac{\pi}{6}$ (T)

I_v and I_w are negative ($\pi/6 \leq \omega_o t \leq \pi/6$), diode d_{u_2}, d_{v_1} and d_{w_1} will begin to conduct. The equivalent circuit is drawn in Fig. 10. The KVL equations for the two loops in this circuit are given by (12) and (13). The KCL equation at node n_i is given by (14).

$$v_v - 2L\frac{d}{dt}i_v - V_{clp} + 2L\frac{d}{dt}i_u - v_u = 0 \tag{12}$$

$$v_w - 2L\frac{d}{dt}i_w - V_{clp} + 2L\frac{d}{dt}i_u - v_u = 0 \tag{13}$$

$$\frac{d}{dt}i_u + \frac{d}{dt}i_v + \frac{d}{dt}i_w = 0 \tag{14}$$

The three equations and three unknowns (12) - (14) can be solved to obtain the rate of change of currents given by (15) - (17).

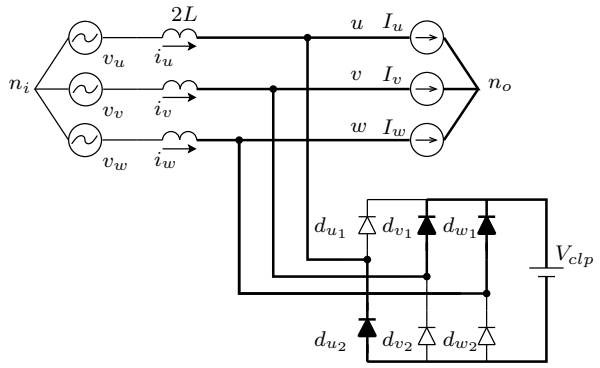

Fig. 10. Zero vector to active vector equivalent circuit

$$\frac{d}{dt}i_u = \frac{3v_u + 2V_{clp}}{6L} \tag{15}$$

$$\frac{d}{dt}i_v = \frac{3v_v - V_{clp}}{6L} \tag{16}$$

$$\frac{d}{dt}i_w = \frac{3v_w - V_{clp}}{6L} \tag{17}$$

The phase currents i_u, i_v and i_w currents flow at the rates defined above until the time one of them reaches the output value. If i_v equals I_v, then, diode d_{v_1} ceases to conduct and i_u and i_w will change at rates given by (18).

$$\frac{d}{dt}i_u = -\frac{d}{dt}i_w = \frac{v_u - v_w + V_{clp}}{4L} \tag{18}$$

During the commutation interval, the difference between the inductor current and output current flows into the the clamp circuit. The associated clamp power loss is given by (19). When I_u and I_v are positive and I_w is negative ($\pi/6 \leq \omega_o t \leq \pi/2$), the clamp power loss is given by (20).

$$\begin{aligned} P_{Clamp} &= V_{clp}(I_u - < i_u >_{t_{ct}}) \\ &= \frac{V_{clp} f_s L}{2}\left[\frac{(I_u - I_w)^2}{v_u - v_w + V_{clp}} - \frac{3I_v^2}{3v_v - V_{clp}}\right] \end{aligned} \tag{19}$$

$$\begin{aligned} P_{Clamp} &= V_{clp}(I_w - < i_w >_{t_{ct}}) \\ &= \frac{V_{clp} f_s L}{2}\left[\frac{(I_u - I_w)^2}{v_u - v_w + V_{clp}} + \frac{3I_v^2}{3v_v + V_{clp}}\right] \end{aligned} \tag{20}$$

The value of V_{clp} is selected to be $5 \times V$. The per unit power loss curves for certain values of output current as $\omega_o t$ is varied from 0 to 2π are plotted in Fig. 11 and Fig. 12. Here again the maximum and minimum clamp power loss is equal to 4.6 and 2.2 p.u. respectively. Table II lists the commutation time

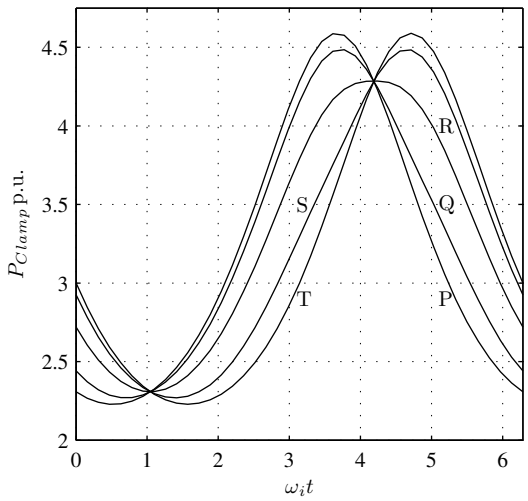

Fig. 12. Clamp circuit power loss : Zero to active vector $\omega_o t$ (rads) = $\frac{\pi}{6}$ (P) , $\frac{\pi}{4}$ (Q), $\frac{\pi}{3}$ (R), $\frac{5\pi}{12}$ (S) and $\frac{\pi}{2}$ (T)

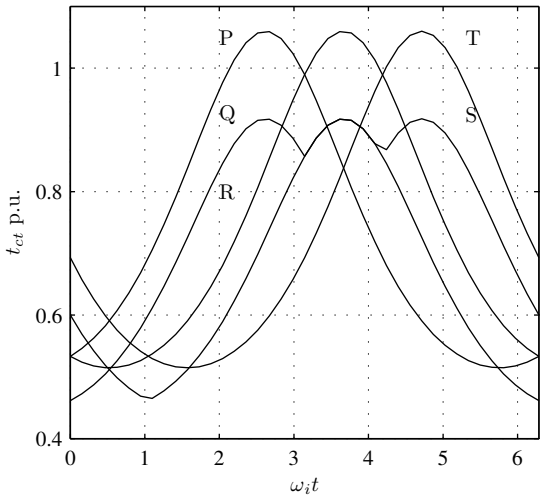

Fig. 13. Commutation time required: Zero to active vector $\omega_o t$ (rads)= $-\frac{\pi}{6}$ (P), 0 (Q) , $\frac{\pi}{6}$ (R), $\frac{\pi}{3}$ (S) and $\frac{\pi}{2}$ (T)

required for a zero to active vector transition. As before, the commutation time required in per unit as a function of input voltage is plotted in Fig. 13. The worst case commutation time required is $1.06LI/V$ sec.

There is some output voltage distortion associated with the clamp circuit operation. During an active to zero vector transition, the clamp circuit voltage does not appear across the load. A voltage loss or distortion occurs only during a zero to active vector transitions. In a worst case situation, the clamp circuit may apply $\pm\frac{2}{3}V_{clp}$ across the output line-neutral of a particular phase for the longest commutation time.

TABLE II
COMMUTATION TIME (ZERO-ACTIVE, S_1 ON)

Transition	time	Total time (t_{ct})
$-\frac{\pi}{6} \leq \omega_o t \leq \frac{\pi}{6}$	$t_v = \frac{6LI_v}{3v_v - V_{clp}}$ $t_w = \frac{6LI_w}{3v_w - V_{clp}}$	$= 2L\frac{(I_u - I_w)}{v_u - v_w + V_{clp}}$ for $t_v \leq t_w$ $= 2L\frac{(I_u - I_v)}{v_u - v_v + V_{clp}}$ otherwise
$\frac{\pi}{6} \leq \omega_o t \leq \frac{\pi}{2}$	$t_v = \frac{6LI_v}{3v_v + V_{clp}}$ $t_u = \frac{6LI_u}{3v_u + V_{clp}}$	$= 2L\frac{(I_u - I_w)}{v_u - v_w + V_{clp}}$ for $t_v \leq t_u$ $= 2L\frac{(I_v - I_w)}{v_v - v_w + V_{clp}}$ otherwise

IV. SIMULATION RESULTS

A. Intervals t_{az1} and t_{za1}

The circuit in Fig. 1 is simulated in SABER for one switching cycle. The input voltages and output currents are dc sources of magnitudes listed in Table III. Fig. 14 is the plot of currents i_a, i_b and i_c when a zero vector is applied and S_1 is ON. The phase currents for the zero to active vector transition when S_1 is ON are shown in Fig. 15. The simulated values for the slope of the current coincide with the calculated values. The clamp circuit power loss during a zero to active vector transition when S_2 is ON (t_{za2}) is equal to the power loss for an active to zero transition when S_1 is ON (t_{az1}) and it is equal to 44 Watt by calculation. The clamp circuit power loss for the transition t_{az2} equals that of t_{za1} equal to 25.74 Watts. The values for commutation time required as well as total clamp power loss in one switching cycle are listed in IV. The calculated values match the simulated values very closely.

TABLE III
SIMULATION PARAMETERS

v_u, v_v,v_w	100 ,-40,-60 V
I_u, I_v , I_w	20, -5,-15 A
V_{clp}	600 V
L	50μ H
Turns ratio	1:1:1

TABLE IV
SIMULATION RESULTS

Value	Simulation	Calculation
P_{clamp}	135.5 W	139.4 W
$t_{az1} = t_{za2}$	8.05μ sec	7.95μsec
$t_{za1} = t_{az2}$	4.62μ sec	4.61μ sec

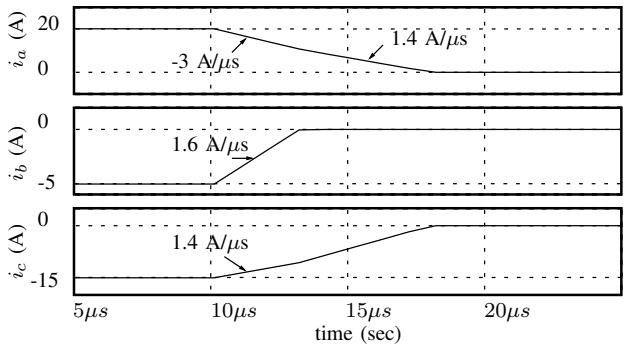

Fig. 14. Active to zero vector simulation results (t_{az1})

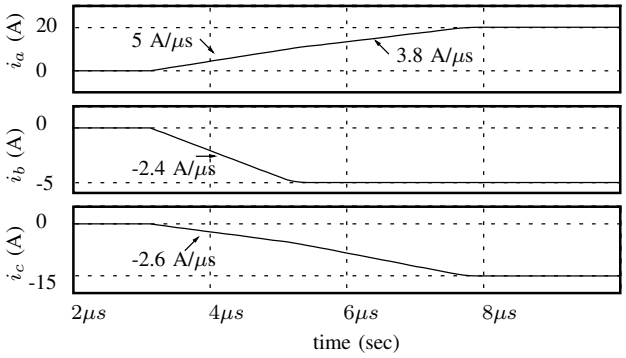

Fig. 15. Zero to active vector simulation results (t_{za1})

TABLE V
SIMULATION PARAMETERS: THREE PHASE SYSTEM

V_i	100V
V_o	30V
ω_i	$2\pi 60$ rad/sec
ω_o	$2\pi 60$ rad/sec
Output power	1kW
Load pf.	0.8
L	12 μH
V_{clp}	500V

B. Three phase ac/ac case for same frequency

A 1kW three phase ac-ac system in Fig. 1 is simulated with the parameters listed in Table V. Where V_i and V_o are the peak values of input and output balanced three phase voltages respectively. The matrix converter is controlled using the technique described in section II. Using this method, unity power factor is obtained on the primary side. The input voltage and filtered input current for phase a and current for phase u are plotted in Fig. 16. The worst case clamp power loss according to the analysis is 81.154 W (8.12 %) and the least clamp power loss is 17.68 W (1.768 %). The clamp power loss from simulation equals 79.89 W (7.99 %). The peak output voltage from simulation is 26.22 Watts, that corresonds to a voltage loss of 3.78 V. This is below the worst prediction of 10.27 V for voltage loss.

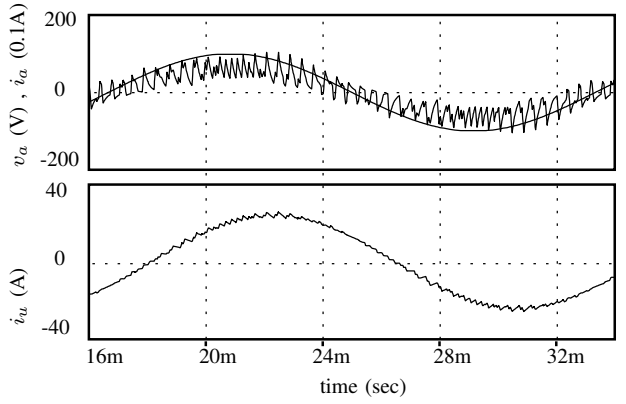

Fig. 16. 1kW, 0.8 pf, three phase ac/ac

C. Three phase variable frequency ac

The same 1kW system is simulated for a reference output voltage of 30V, 120 Hz. The output current and filtered input current along with input voltage for one phase are plotted in Fig. 17. The simulated values of power loss and voltage loss are within the calculated limits.

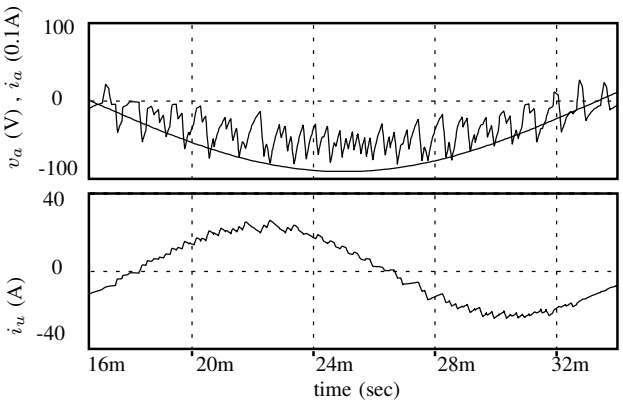

Fig. 17. 1kW, 0.8 pf, three phase variable frequency 60Hz - 120Hz

V. CONCLUSION

In this paper, the clamp circuit requirement is studied and a detailed analysis of its operation is done. The lower and upper limit of power loss associated with the leakage energy commutation using a clamp circuit is calculated and these values are checked with the simulated values. The following conclusions can be drawn,

1) The value of clamp voltage must be greater than three times the peak line to neutral voltage.
2) The clamp circuit is operational every time the load side converter is switched.
3) For $V_{clp} = 5 \times V$, the power loss associated with it is between $4.46 f_s L I^2$ and $9.18 f_s L I^2$ Watts.
4) For $V_{clp} = 5 \times V$, the maximum time required for commutation can be upto $1.06 \times LI/V$ sec .
5) Zero to active vector transitions in the load side converter lead to distortion in the output voltage waveform.

The results of this analysis can be used to design the resistive and capacitive components for the clamp circuit. This analysis is very general and can be further extended to the clamp circuit operation in any other topology.

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